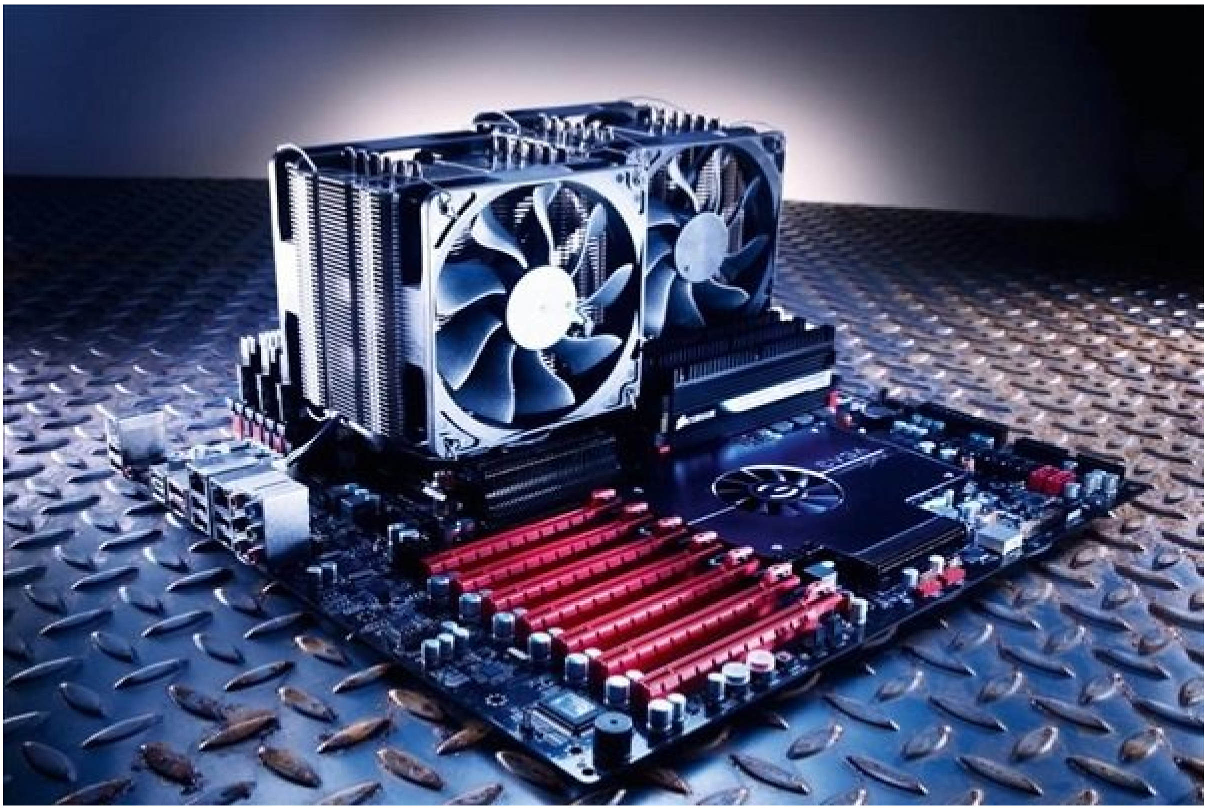
[illegible]

CHIPS: [illegible]



[illegible] CHIPS [illegible] RISC-V [illegible]

[illegible] 2019 [illegible] CHIPS Alliance [illegible] Common Hardware for Interfaces, Processors and Systems [illegible]

[illegible]

[illegible]

[illegible] CHIPS [illegible] CHIPS [illegible] CHIPS [illegible] CHIPS [illegible]

[illegible] RISC-V

[illegible] CHIPS [illegible] (Esperanto)، [illegible] (SiFive) [illegible] (Western Digital) [illegible] RISC-V [illegible] RISC-V [illegible] CHIPS [illegible] CHIPS [illegible] CHIPS [illegible] RISC-V. [illegible] RISC-V [illegible] ([illegible] [[illegible] RISC-V [illegible]]). [illegible] RISC-V، [illegible] CHIPS [illegible] CHIPS [illegible] RISC-V [illegible] RISC-V [illegible].

[illegible] RISC-V [illegible]. [illegible] Wave Computing [illegible] RISC-V [illegible] MIPS [illegible] RISC-V [illegible] FOSSi ([illegible] LibreCores، Free and Open Source Silicon)، OpenCores [illegible].

[illegible]

[illegible] CHIPS [illegible] (design verification) [illegible].

[illegible]: «[illegible].» [illegible]. [illegible] CHIPS [illegible].

[illegible]: « [illegible].»

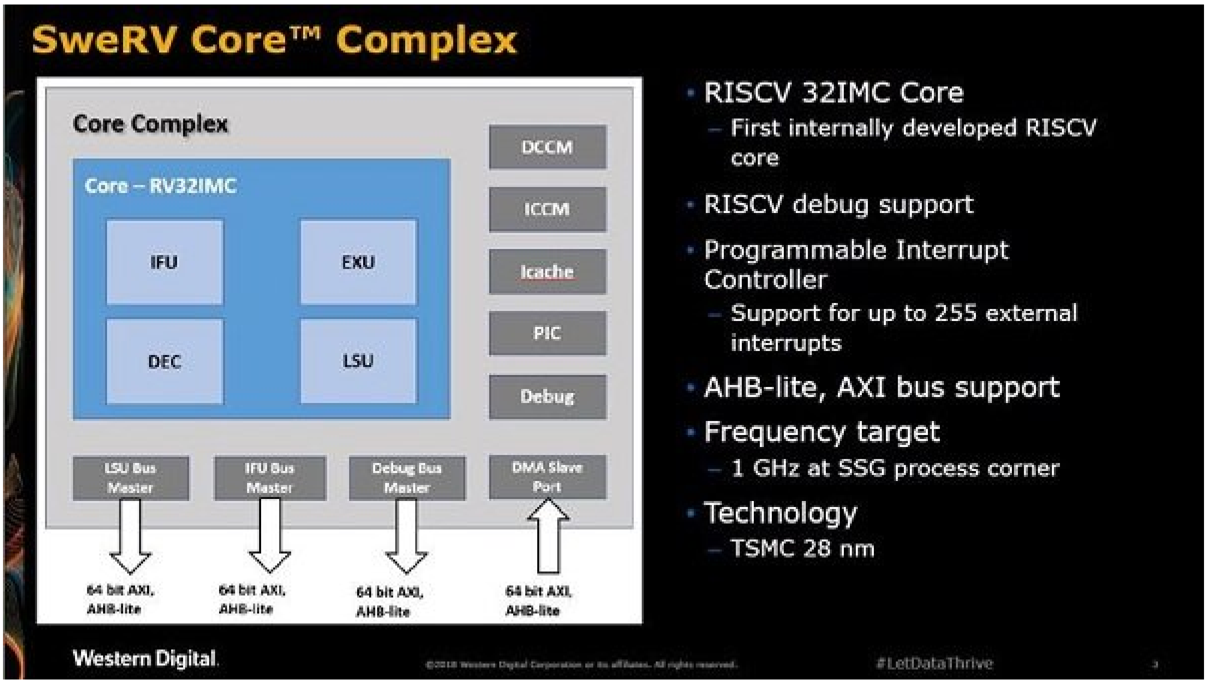
[illegible] (Martin Fink) [illegible] RISC-V [illegible].

[illegible]: « [illegible] CHIPS [illegible].»

[illegible]: «CHIPS [illegible] (data-centric) [illegible].» [illegible]: « [illegible] CHIPS [illegible].» [illegible].

CHIPS [illegible]

[illegible] RISC-V [illegible]. [illegible] SweRV [illegible].

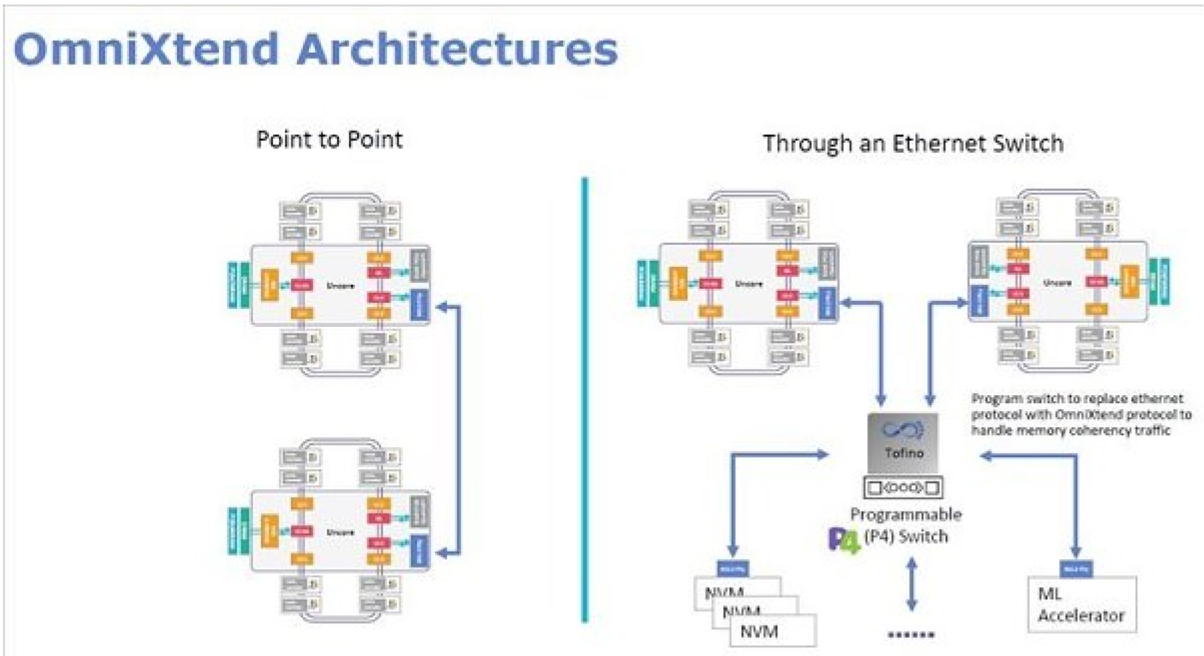


SweRV Core™ Complex

- RISCV 32IMC Core
  - First internally developed RISCV core
- RISCV debug support
- Programmable Interrupt Controller
  - Support for up to 255 external interrupts
- AHB-lite, AXI bus support
- Frequency target
  - 1 GHz at SSG process corner
- Technology
  - TSMC 28 nm

□□□□ □□□□ *CHIPS* □□□□□□ □□ □□ *RISC-V* □□ □□□□□ *SweRV* □□□□ □□ □□□□□□□ □□□□□□□□□□□□□□ □□□□ - □□□□ .□□□

□□ (2 □□□□) OmniXtend □□□□□□ □(1 □□□□) SweRV □□□□ □□ □□□□□□□ □□ □□□□□ □□□□ □□□ □□ □□□□□□□□□□□□ □□ □□□□□ □□□□□□□□ □ □□□ □□□□□□□□ SweRV □□ □□□□□□ CHIPS □□□□ □□□□.



OmniXtend Architectures

Point to Point
Through an Ethernet Switch
Uncore
Tofino
Programmable (P4) Switch
Program switch to replace ethernet protocol with OmniXtend protocol to handle memory coherency traffic
NVM
NVM
NVM
ML Accelerator
......

□□□□ *CHIPS* □□□□□□ □□ □□□□□□□□□□□□ □□ □□□□ *OmniXtend* □□□□□□ □□ □□□□□□□□ □□□□□ *CXL* - □□□□ .□□□ □□□□

□□□□ □□ □□□□ □□□□ □□□ □ □□□□□ □□□ □□□□□ CHIPS □□□□□□□ □□ □□□□ □□□□ □□ □□□□ □□□□□ □□□□ □□ CXL □□□□□□ □□□□□ □ □□□□ □□□□□□□ □□□ □□ □□ Compute Express Link □□□□□ CXL □□□□□□□□ □□□□□ □□ OmniXtend □□□□□□ □□ □□□□□ □□□□ CXL □□ □□□□□□ □ □□□□□□□ □□ □□□□□□ .□□□□□□□□ □□□ □□ □□□□□ .□□□ □□□□□ □□□□ □□□□ CHIPS □□□□□□ □□ □□□□□□□□□□□□

□□□□□□ □□ □□□ □□□□□□ □□□□□ RISC-V □□□□□□□ □ □□□□□□ □□□□□□ □□□□□□□□□□□□ □□□□ □□ SiFive □□□□ □□□□□□□□ □□□□□ □□□□ □□ □□□ □ RISC-V □□ □□□□□ □□□□□□□ □□□□□□□□□□□□□□ □□□□□□ □□□□□□ □□□□□□□ RocketChip SoC □□□□□ □□□ □□□□ □□□□□ □□ □□□□□□ □□□ .□□□□□□□ □□□□□ □□ Chisel □□□□□ □□□□□□□ CHIPS □□ □□□□ □□□□□□□ SiFive .□□□ □□□□□□ TileLink coherent interconnect fabric □ generator [illegible] Microchip [illegible] CHIPS [illegible] PolarFire [illegible] U54-MC [illegible] SiFive [illegible] PolarFire [illegible] FPGA SOC [illegible] RISC-V [illegible] UVM [illegible] Universal Verification Methodology [illegible]

[illegible]

[illegible]

[illegible]:
https://www.linux.com/tutorials/chips-alliance-create-open-chip-design-tools-risc-v-and-beyond/
https://www.linuxfoundation.org/press-release/2019/03/linux-foundation-to-host-chips-alliance-project-to-propel-industry-innovation-through-open-source-cpu-chip-and-soc-design/

[illegible]:
[illegible]
[illegible]:
[illegible]
[illegible]:
11:30 - 20/11/1398
[illegible]:
CHIPS - [illegible]

[illegible]
[illegible]: https://www.shabakeh-mag.com/information-feature/16550/chips-%D8%A7%D8%AA%D8%AD%D8%A7%D8%AF%DB%8C-%D8%A7%D9%BE%D9%86%E2%80%8C%D8%B3%D9%88%D8%B1%D8%B3-%D8%A8%D8%B1%D8%A7%DB%8C-%D8%AA%D9%88%D8%B3%D8%B9%D9%87-%D8%B3%D8%AE%D8%AA%E2%80%8C%D8%A7%D9%81%D8%B2%D8%A7%D8%B1