禪

[illegible]

[illegible] :RISC-V

[illegible]

[illegible] **RISC-V** [illegible]

[illegible]

[illegible].
[illegible] ASIC [illegible] (SoC) [illegible] ARM [illegible] MIPS [illegible] 1[illegible] [illegible] (validation) [illegible] SoC [illegible] ISA [illegible] ISA [illegible] **RISC-V** [illegible].

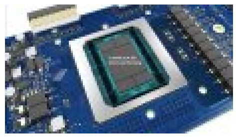
[illegible] RISC-V

RISC-V [illegible] (ISA) [illegible] **RISC-V** [illegible]. [illegible] ARM [illegible]. RISC-V [illegible] BSD [illegible] embedded [illegible].
RISC-V[illegible] RISC [illegible] ARM [illegible] PowerPC [illegible] x86 [illegible] ISA [illegible] ISA [illegible] RISC-V [illegible].
[illegible] (SoC) [illegible] (GitHub) [illegible] ARM [illegible] **RISC-V** [illegible] NXP[illegible] GlobalFoundries [illegible] UltraSoC [illegible]. ([illegible])

[illegible]

[illegible] RISC-V [illegible] (instruction set) [illegible] RISC-V [illegible] (Western Digital) [illegible] AMD [illegible] x86 [illegible] ARM [illegible] ARM [illegible]

[illegible]



[illegible]

[illegible]

[illegible] ARM [illegible] RISC-V

[illegible] **ARM** [illegible] «[illegible] RISC-V: [illegible]» ([illegible] RISC-V Architecture: Understand the Facts) [illegible] **RISC-V** [illegible] ARM [illegible] RISC-V [illegible] **ARM** [illegible] ARM [illegible]

ARM [illegible] ARM [illegible] RISC-V [illegible] ARM [illegible] RISC-V [illegible] ARM [illegible] ARM [illegible] ARM [illegible] RISC-V [illegible] **ARM** [illegible] ARM [illegible] RISC-V [illegible] **ARM** [illegible] RISC-V [illegible] **ARM** [illegible] (Acorn [illegible]) [illegible] ARM [illegible] ARM [illegible] Spectre [illegible] Meltdown [illegible]

[illegible] (Miguel de Icaza) [illegible] «[illegible]» (GNOME) [illegible] ARM [illegible] RISC-V [illegible] ARM [illegible] **ARM** [illegible]

[illegible] arm-basics.com [illegible] ARM [illegible] ARM [illegible] arm-basics.de [illegible]

[illegible] ARM [illegible].

[illegible] RISC-V [illegible]

[illegible] ISA [illegible] TIRIAS Research [illegible] SiFive [illegible] ISA [illegible]

	Custom ISA	Licensed ISA	Licensed ISA with architecture license	Open-Source ISA
Design Flexibility	High	Low	Moderate to high	High
License Fees	None	$0 to millions	$0 to millions	None
Royalty Fees	None	0 to a few %	0 to a few %	0 to a few %
Available Software	None to little	Moderate to extensive	Moderate to extensive	Little to moderate
Processor Cores	Custom	Standard	Standard to custom	Custom or standard
Hardware Engineering Costs	High	Low	Low to moderate	High
Software Engineering Costs	High	Low to moderate	Low to moderate	Moderate to high
Development Time	Long	Short	Short to moderate	Long
Manufacturability Risk	High	Low	Low to moderate	Moderate to high
Time-to-Market	Long	Short	Short to moderate	Moderate to high

[illegible] (sets) [illegible] mask set [illegible] mask) [illegible]

[illegible] **RISC-V** [illegible] (firmware) [illegible] **ARM** [illegible] x86 [illegible] ISA [illegible] ARM [illegible]

[illegible]

[illegible]

[illegible] RISC-V

[illegible] Krste Asanovic [illegible] SiFive [illegible] RISC-V [illegible] (storage controller) [illegible] ISA [illegible] Asanovic. [illegible] RISC-V [illegible] SiFive [illegible] (licensable) [illegible] (custom) [illegible].

[illegible] mask [illegible] set[illegible]: «[illegible] **ISA** [illegible].» [illegible]

[illegible] ISA [illegible].

[illegible] RISC-V

[illegible] RISC-V [illegible] **RISC-V** [illegible]

[illegible] Asanovic [illegible]: «[illegible] SoC [illegible] DRAM [illegible] Asanovic [illegible]: «[illegible] SiFive [illegible] RISC-V [illegible] SoC [illegible] SoC [illegible].» [illegible]

[illegible] RISC-V

[illegible] RISC-V [illegible] ISA [illegible]

[illegible] ISA [illegible]

[illegible] SoC [illegible]

[illegible] **RISC-V** [illegible]

[illegible] RISC-V [illegible]

[illegible] Cortex-A [illegible] **ARM** [illegible] **ARM** [illegible]

[illegible] **RISC-V** [illegible]

[illegible]:

[illegible]

[illegible]:

RISC-V's Open-Source Architecture Shakes Up Chip Design

Arm kills off its anti-RISC-V smear site after own staff revolt

11 Myths About the RISC-V ISA

RISC-V Gains Its Footing

Here are ARM's biggest anti-RISC-V arguments and why they don't make sense

The Difference Between ARM, MIPS, x86, RISC-V And Others In Choosing A Processor Architecture

[illegible]:

[illegible]

[illegible]

[illegible]:

18/07/1397 - 13:10

[illegible]:

RISC-V - [illegible] - [illegible] - [illegible] - ARM - [illegible] - [illegible]

[illegible]

[illegible]: https://www.shabakeh-mag.com/hardware/13880/risc-v-%D9%BE%D8%A7%D8%B3%D8%AE-%D8%A7%D9%BE%D9%86%E2%80%8C%D8%B3%D9%88%D8%B1%D8%B3-%D8%A8%D9%87-%DA%86%D8%A7%D9%84%D8%B4%E2%80%8C%D9%87%D8%A7%DB%8C-%D8%B5%D9%86%D8%B9%D8%AA-%D8%AA%D8%B1%D8%A7%D8%B4%D9%87