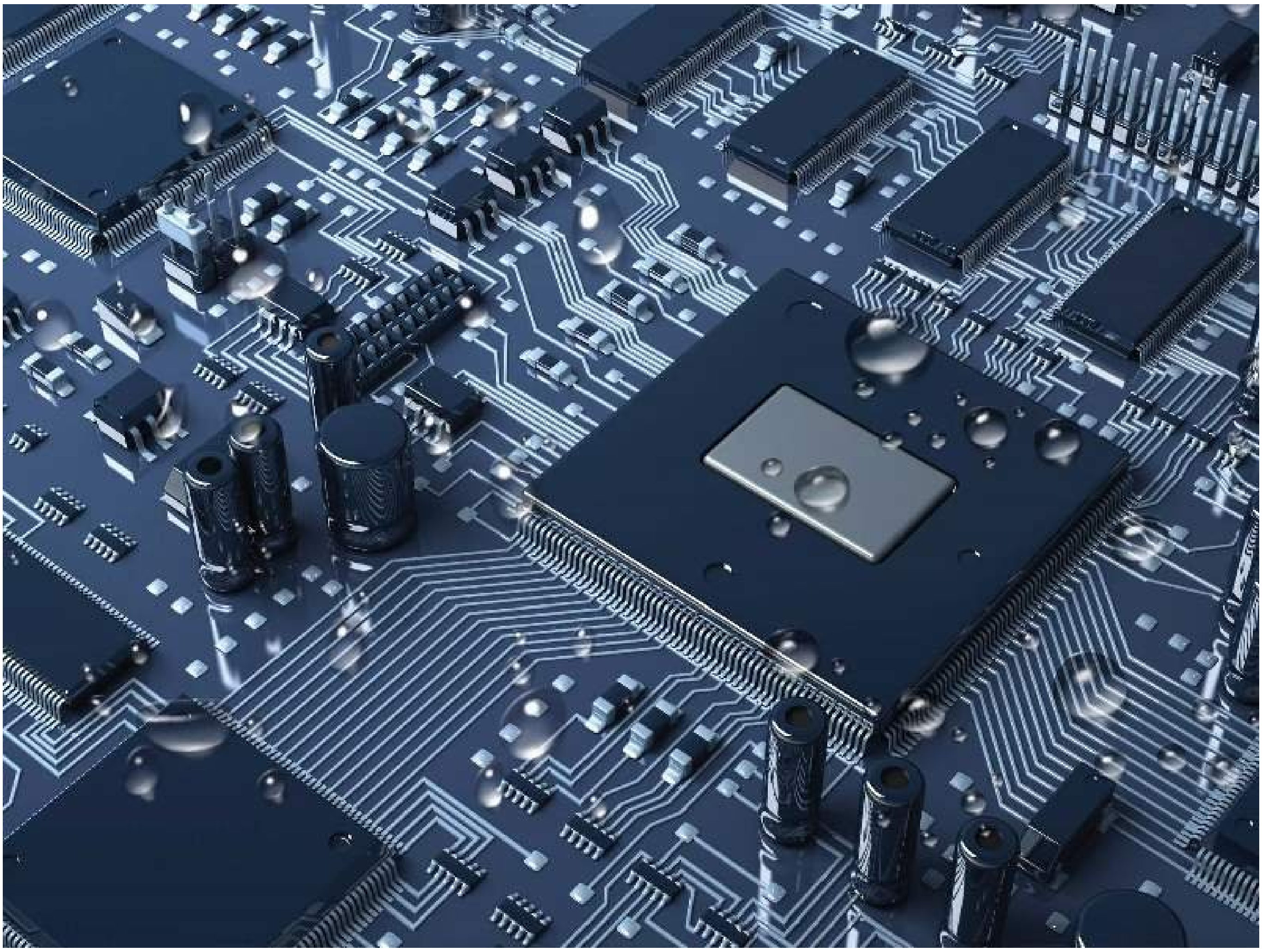
禪

# [illegible]



[illegible]

[illegible]

[illegible] UNIVAC I [illegible] «[illegible]» [illegible] «[illegible]» [illegible] (10 [illegible] 1 [illegible]) [illegible]

## [illegible]

[illegible]

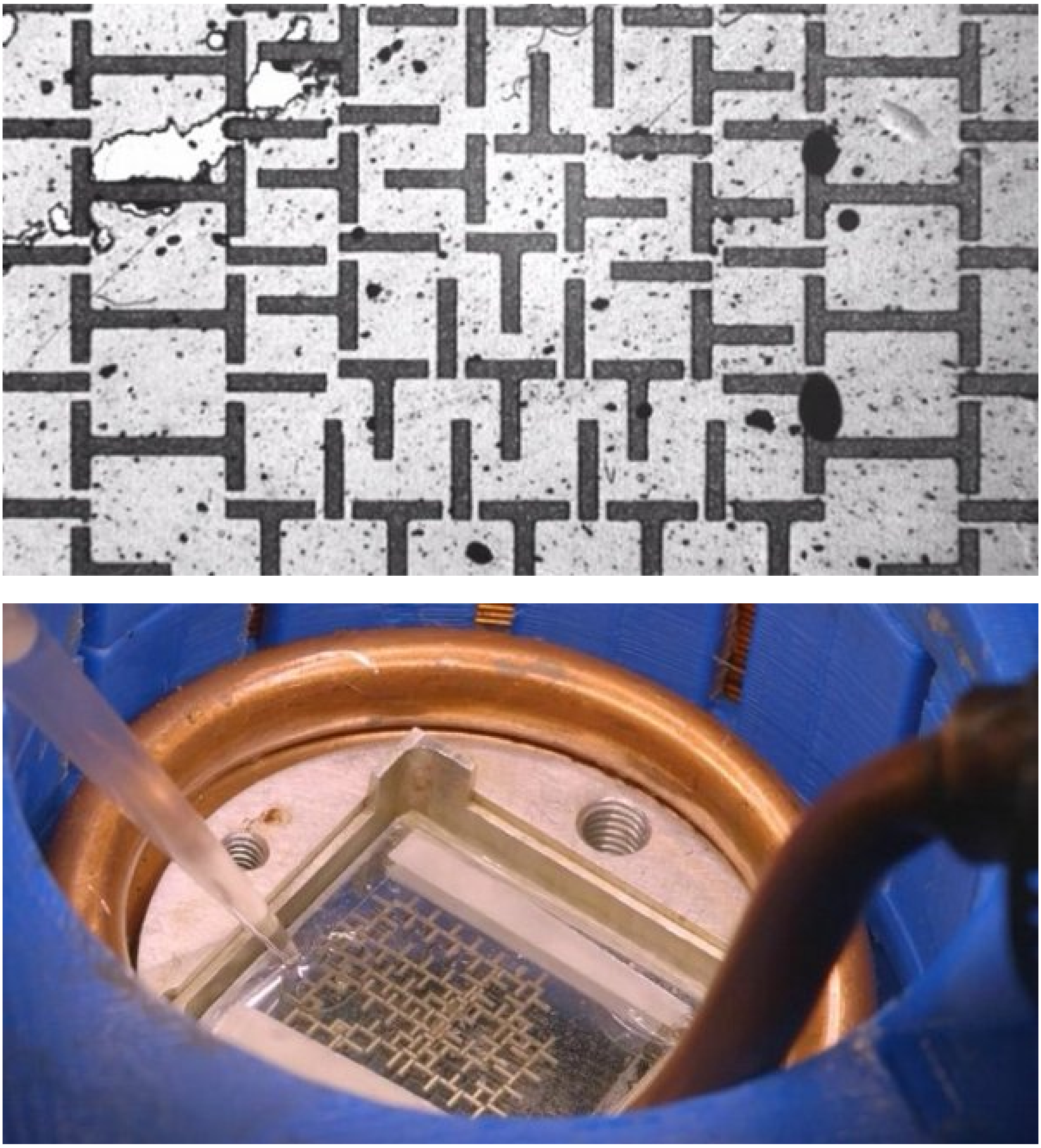
[illegible] «[illegible]» (Computer clock) [illegible] ([illegible]) [illegible]

## [illegible]

[illegible] «[illegible]» [illegible]

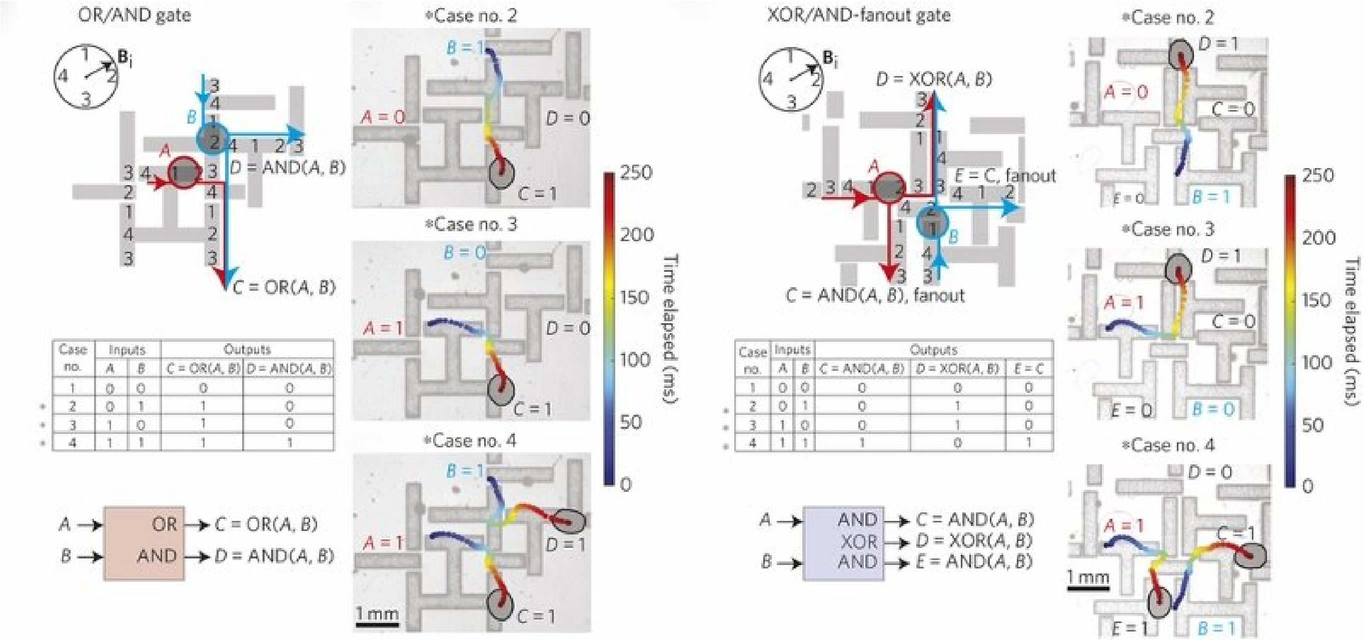
## [illegible]

[illegible] T [illegible] I [illegible] (1 [illegible]) [illegible]



[illegible] 1 [illegible]: [illegible] T [illegible] I [illegible].
[illegible]: [illegible].

[illegible] OR [illegible]. [illegible] OR [illegible] (2 [illegible]).



| Case no. | Inputs A | Inputs B | Outputs C = OR(A, B) | Outputs D = AND(A, B) |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 |
| * 2 | 0 | 1 | 1 | 0 |
| * 3 | 1 | 0 | 1 | 0 |
| * 4 | 1 | 1 | 1 | 1 |

| Case no. | Inputs A | Inputs B | Outputs C = AND(A, B) | Outputs D = XOR(A, B) | Outputs E = C |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 |
| * 2 | 0 | 1 | 0 | 1 | 0 |
| * 3 | 1 | 0 | 0 | 1 | 0 |
| * 4 | 1 | 1 | 1 | 0 | 1 |

*[illegible] 2 [illegible]:*

*1- [illegible] OR [illegible] AND: [illegible] A ([illegible]) [illegible] B ([illegible]) [illegible]. [illegible].*
*[illegible] A [illegible].*

*2- [illegible] OR [illegible] AND*

*3- [illegible]*

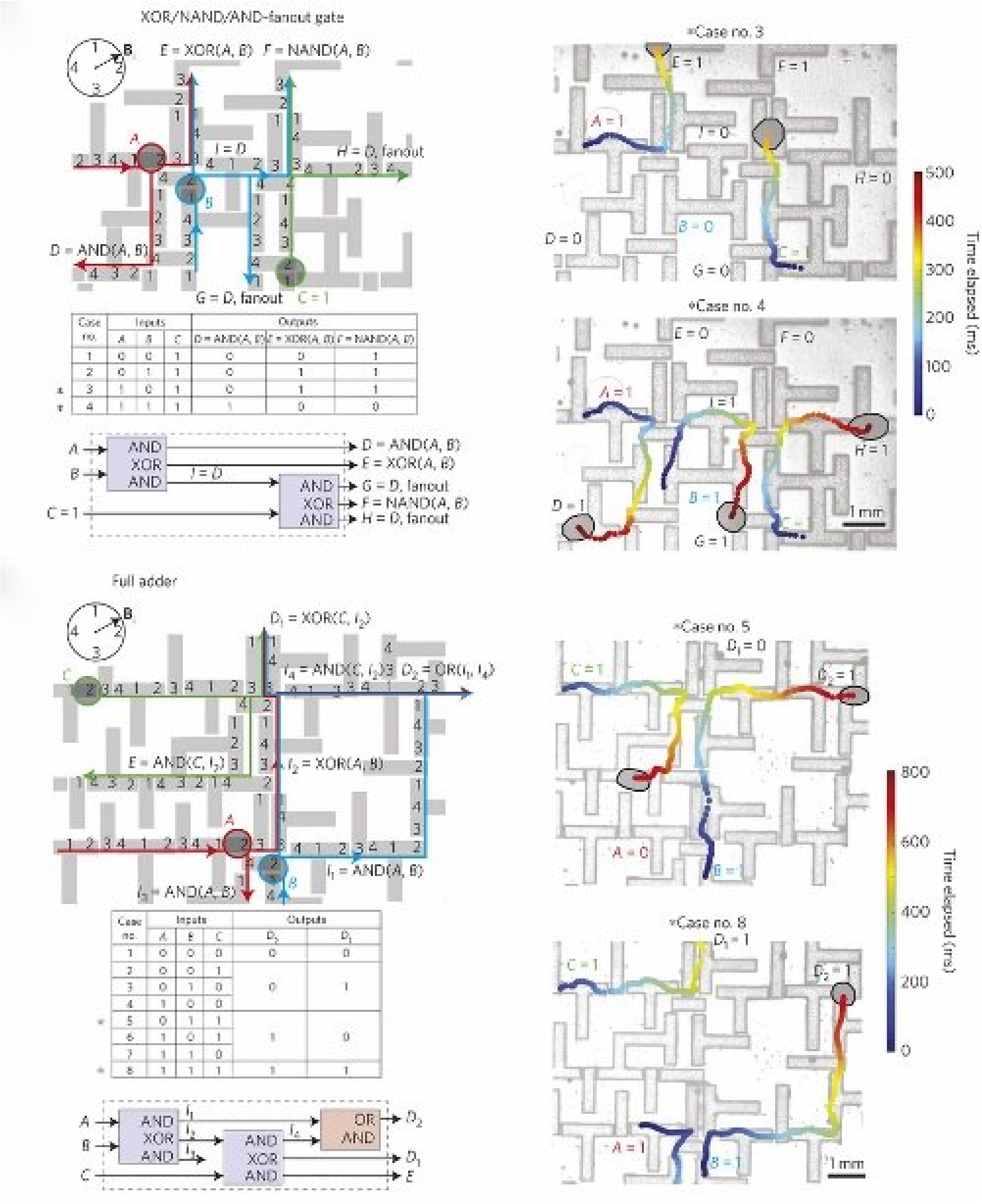
*4- [illegible] A=0 [illegible] B=1 [illegible] B [illegible] [illegible]*
*[illegible] B [illegible] C ([illegible] OR). [illegible]*
*C=1 [illegible] D ([illegible] AND) [illegible] D=0 [illegible].*

*5- [illegible] A=1 [illegible] B= 0 [illegible] OR [illegible]. [illegible] C=1 [illegible] D=0 [illegible].*

*6- [illegible] OR [illegible] AND [illegible].*

*[illegible]: XOR ([illegible])*

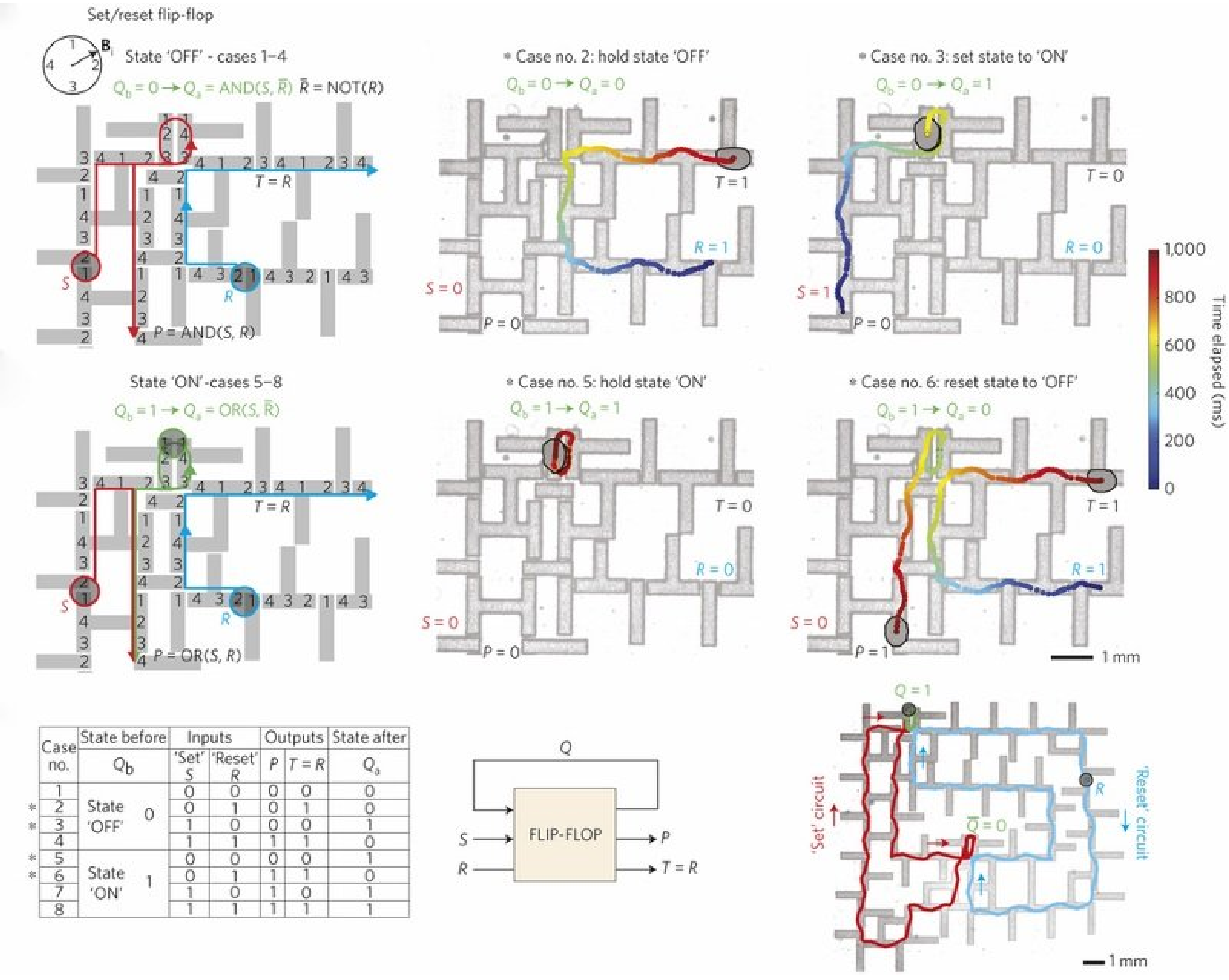
[illegible] AND[illegible] OR [illegible] XOR [illegible] ([illegible] 3 [illegible] 4). [illegible].


XOR/NAND/AND-fanout gate
E = XOR(A, B)
F = NAND(A, B)
I = D
H = D, fanout
D = AND(A, B)
G = D, fanout
C = 1
Case no. 3
Case no. 4
Time elapsed (ms)
500
400
300
200
100
0
1 mm
AND
XOR
AND
Full adder
D1 = XOR(C, I2)
I4 = AND(C, I2)
D2 = OR(I1, I4)
E = AND(C, I2)
I2 = XOR(A, B)
I1 = AND(A, B)
I3 = AND(A, B)
Case no. 5
Case no. 8
800
600
400
200
0
OR
AND

[illegible] :3 [illegible]

[illegible]

[illegible]


Set/reset flip-flop
State 'OFF' - cases 1–4
$Q_b = 0 \rightarrow Q_a = \mathrm{AND}(S, \bar{R})$ $\bar{R} = \mathrm{NOT}(R)$
T = R
P = AND(S, R)
State 'ON'-cases 5–8
$Q_b = 1 \rightarrow Q_a = \mathrm{OR}(S, \bar{R})$
P = OR(S, R)
* Case no. 2: hold state 'OFF'
$Q_b = 0 \rightarrow Q_a = 0$
* Case no. 3: set state to 'ON'
$Q_b = 0 \rightarrow Q_a = 1$
* Case no. 5: hold state 'ON'
$Q_b = 1 \rightarrow Q_a = 1$
* Case no. 6: reset state to 'OFF'
$Q_b = 1 \rightarrow Q_a = 0$
S = 0
S = 1
R = 0
R = 1
T = 0
T = 1
P = 0
P = 1
Time elapsed (ms)
1,000
800
600
400
200
0
1 mm
FLIP-FLOP
Q
S
R
P
T = R
Q = 1
$\bar{Q} = 0$
'Set' circuit
'Reset' circuit
1 mm

| Case no. | State before | | Inputs | | Outputs | | State after |
|---|---|---|---|---|---|---|---|
| | $Q_b$ | | 'Set' S | 'Reset' R | P | T = R | $Q_a$ |
| 1 | State 'OFF' | 0 | 0 | 0 | 0 | 0 | 0 |
| * 2 | | | 0 | 1 | 0 | 1 | 0 |
| * 3 | | | 1 | 0 | 0 | 0 | 1 |
| 4 | | | 1 | 1 | 1 | 1 | 0 |
| * 5 | State 'ON' | 1 | 0 | 0 | 0 | 0 | 1 |
| * 6 | | | 0 | 1 | 1 | 1 | 0 |
| 7 | | | 1 | 0 | 1 | 0 | 1 |
| 8 | | | 1 | 1 | 1 | 1 | 1 |

[illegible] *4:* [illegible]

[illegible]. [illegible]. [illegible]: «[illegible].»

## [illegible]

[illegible]: «[illegible].» [illegible]. [illegible] Computing [illegible].

[illegible]:

-http://news.stanford.edu/news/2015/june/computer-water-drops-060815.html
-http://www.nature.com/nphys/journal/v11/n7/full/nphys3341.html
-http://www.wired.co.uk
-http://www.extremetech.com
-http://www.sciencealert.com

[illegible]:

[illegible] [illegible]

[illegible] [illegible]:

[illegible]

[illegible] [illegible]:

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[illegible]:

[illegible] [illegible] [illegible] - [illegible] [illegible] - [illegible] [illegible] - [illegible]

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[illegible] [illegible]:https://www.shabakeh-mag.com/are-network/2270