



The diagram shows a horizontal row of 10 square cells, each representing a bit in a shift register. The cells are arranged in two groups of five. The first group (left) contains five cells, and the second group (right) contains five cells. There is a gap between the two groups. Above the first group, there is a label '5' and a small square box. Above the second group, there is a label '5' and a small square box. The cells are connected by lines, indicating a shift register structure.

[%DA%A9%D9%85%DB%8C%D8%B3%DB%8C%D9%88%D9%86-%D8%B4%D8%A8%DA%A9%D9%87-%D8%B3%D8%A7%D8%B2%D9%85%D8%A7%D9%86-%D9%86%D8%B5%D8%B1-%D8%A7%D8%B3%D8%AA%D8%A7%D9%86-%D8%AA%D9%87%D8%B1%D8%A7%D9%86-%D8%B4%D8%AF](#)